Fig. 1

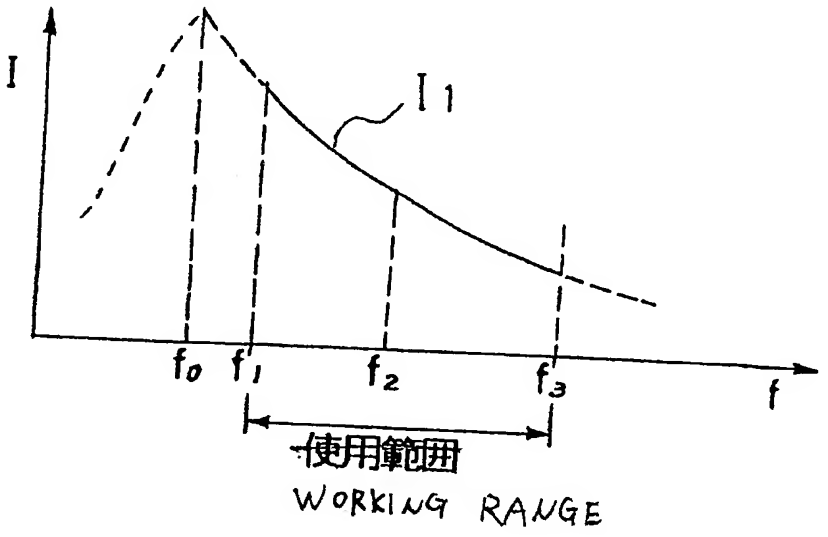


Fig 2

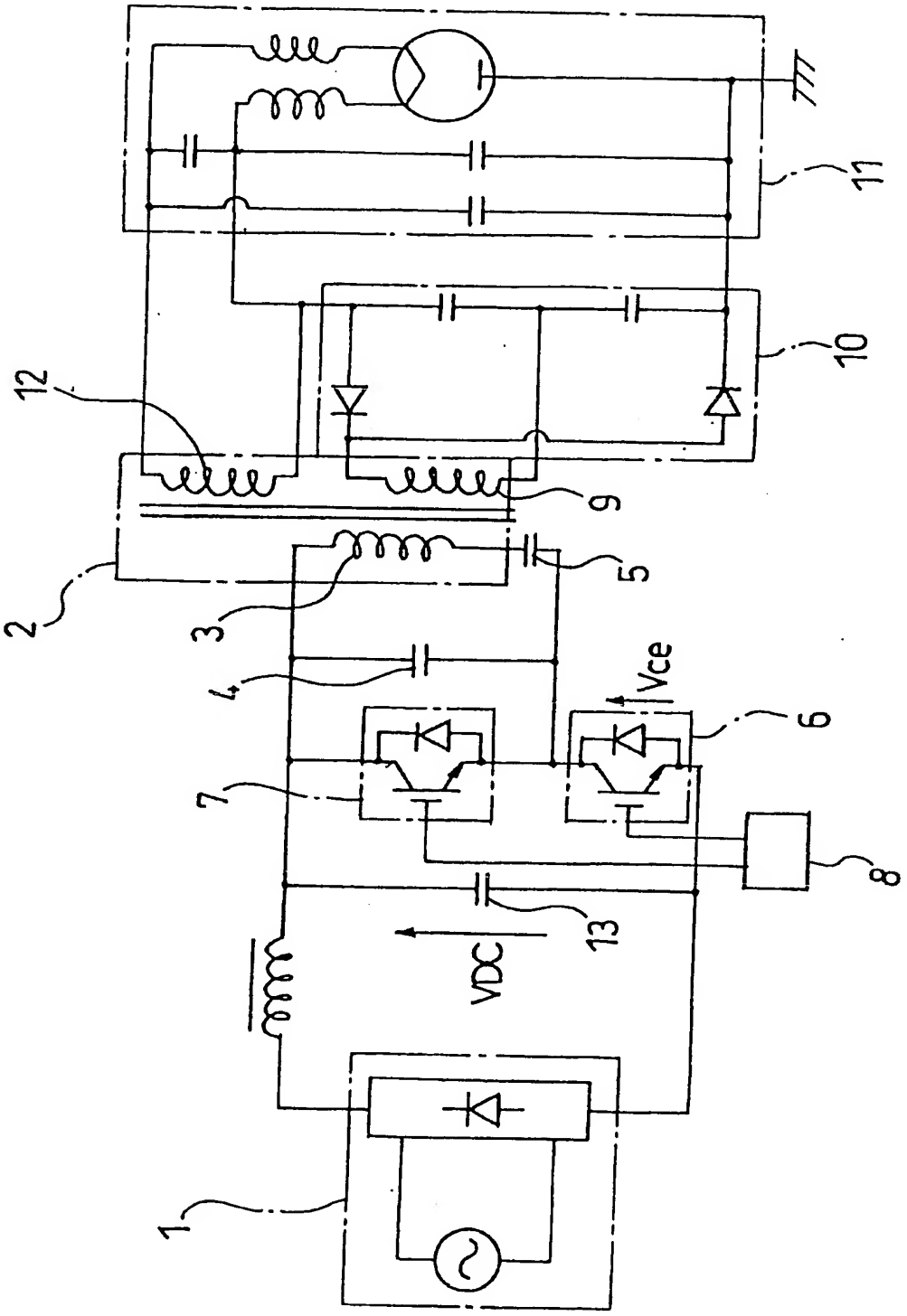


Fig. 3

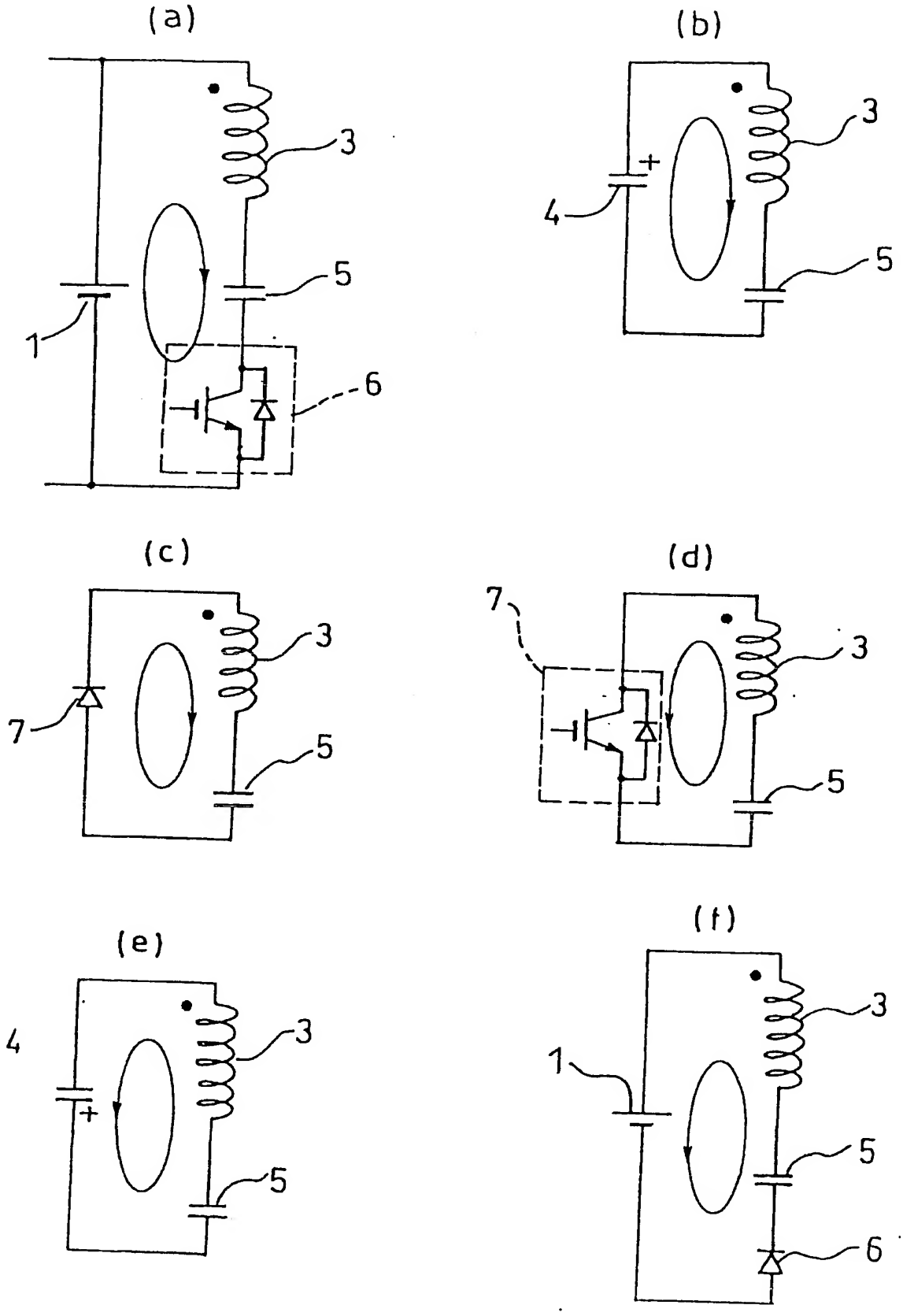


Fig. 4

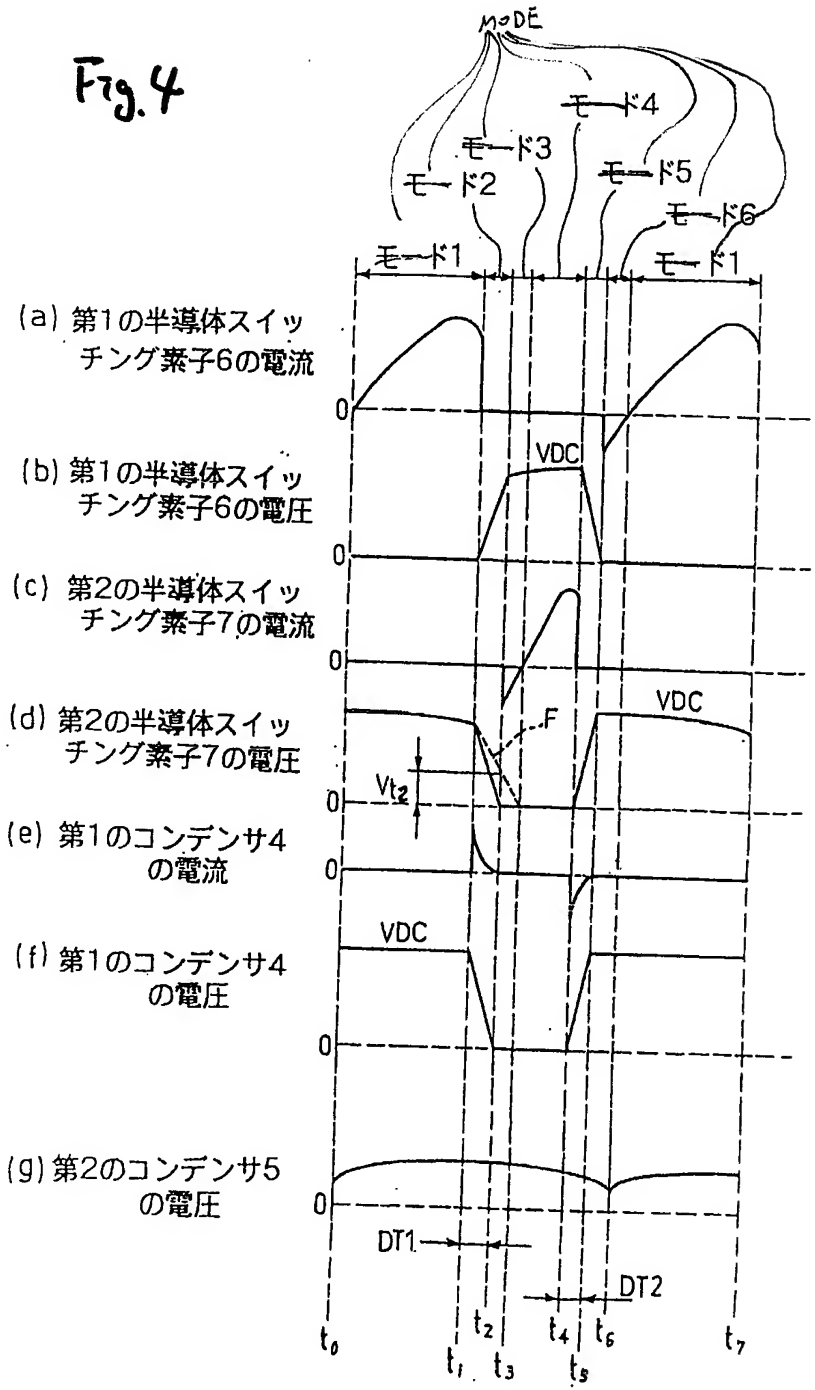


FIG. 4

(a) CURRENT OF FIRST SEMICONDUCTOR SWITCHING DEVICE 6

(b) VOLTAGE OF FIRST SEMICONDUCTOR SWITCHING DEVICE 6

(c) CURRENT OF SECOND SEMICONDUCTOR SWITCHING DEVICE 7

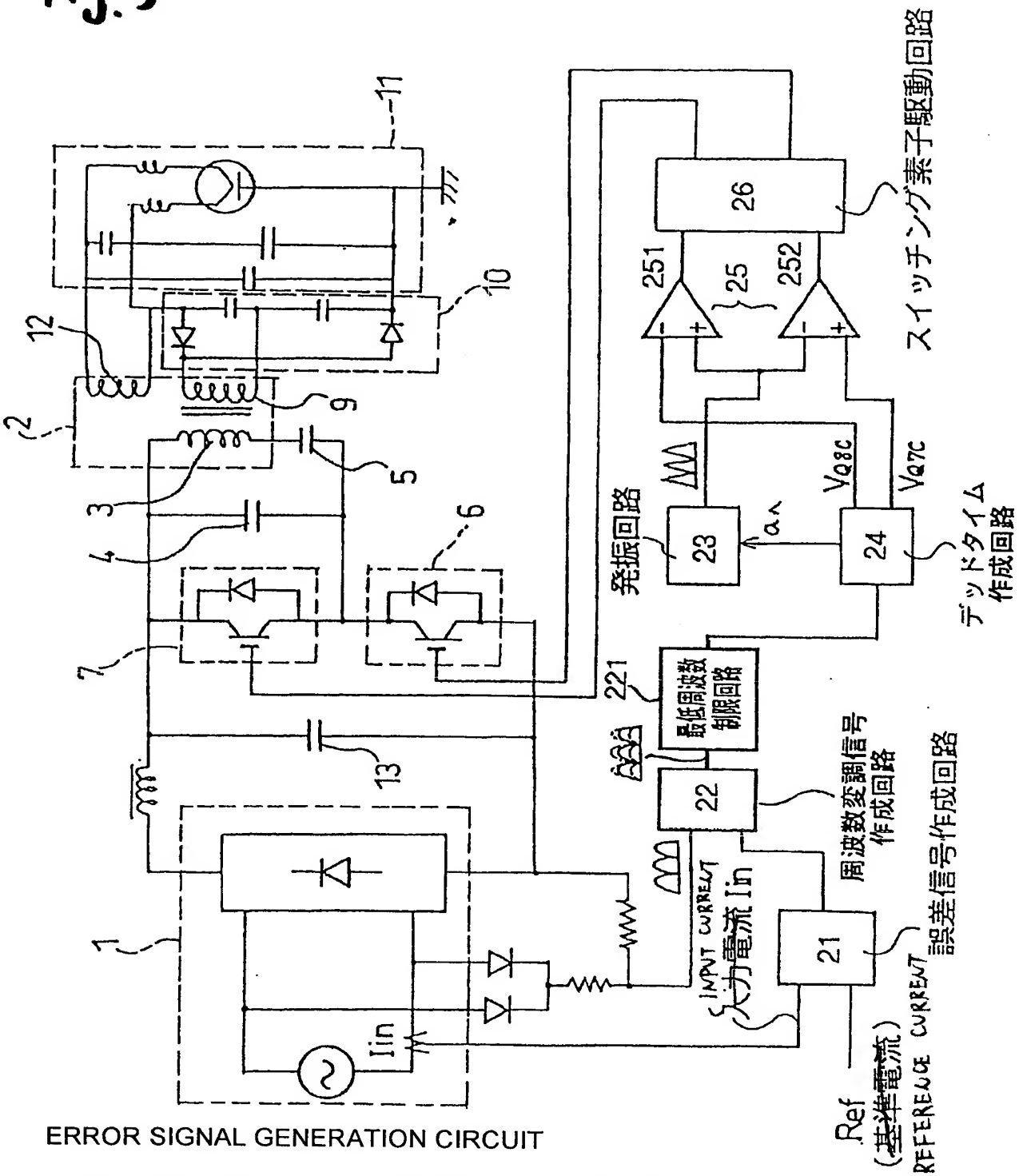
(d) VOLTAGE OF SECOND SEMICONDUCTOR SWITCHING DEVICE 7

(e) CURRENT OF FIRST CAPACITOR 4

(f) VOLTAGE OF FIRST CAPACITOR 4

(g) VOLTAGE OF SECOND CAPACITOR 5

Fig. 5



21 ERROR SIGNAL GENERATION CIRCUIT

22 FREQUENCY-MODULATED SIGNAL GENERATION CIRCUIT

221 LOWEST FREQUENCY LIMITING CIRCUIT

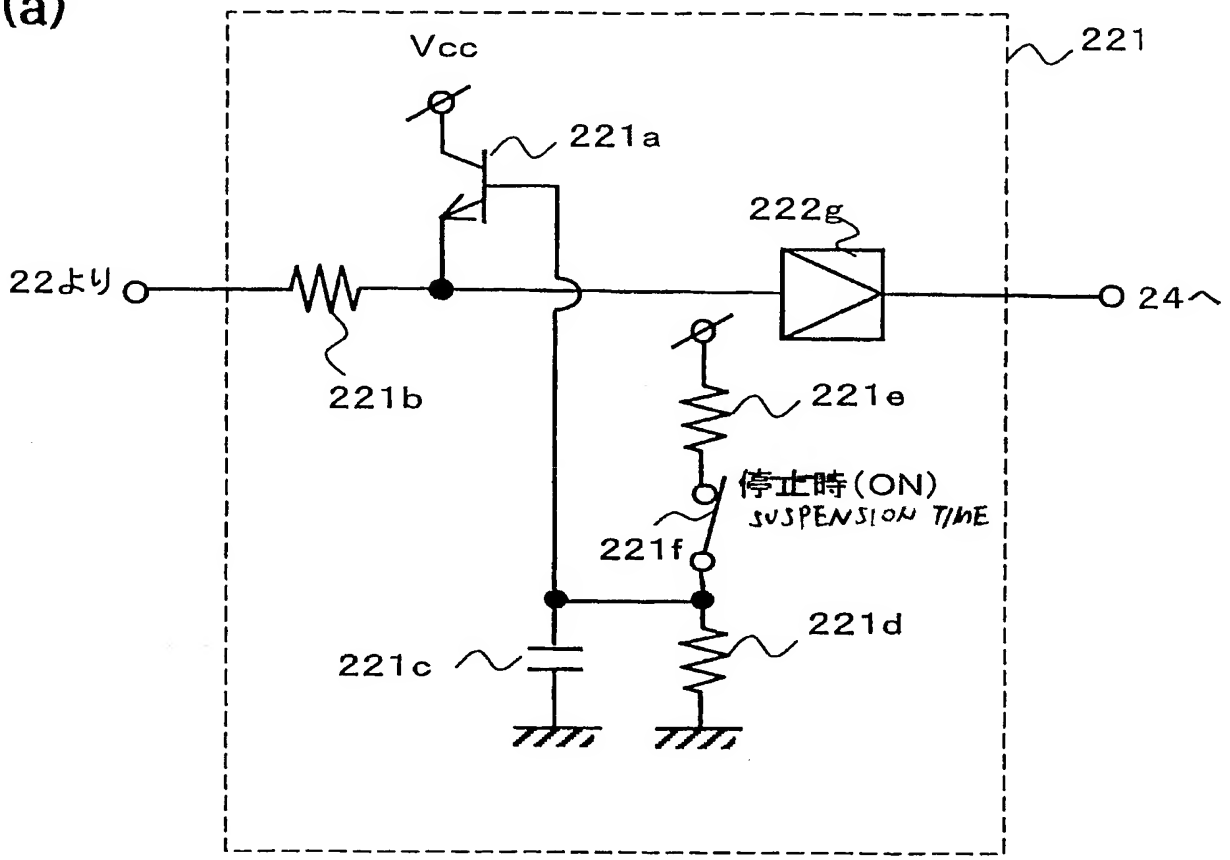
23 OSCILLATION CIRCUIT

24 DEAD TIME GENERATION CIRCUIT

26 SWITCHING DEVICE DRIVE CIRCUIT

Fig. 6

(a)


Vcc
221
221a
222g
22より
24へ
221b
221e
停止時(ON)
SUSPENSION TIME
221f
221d
221c

(b)

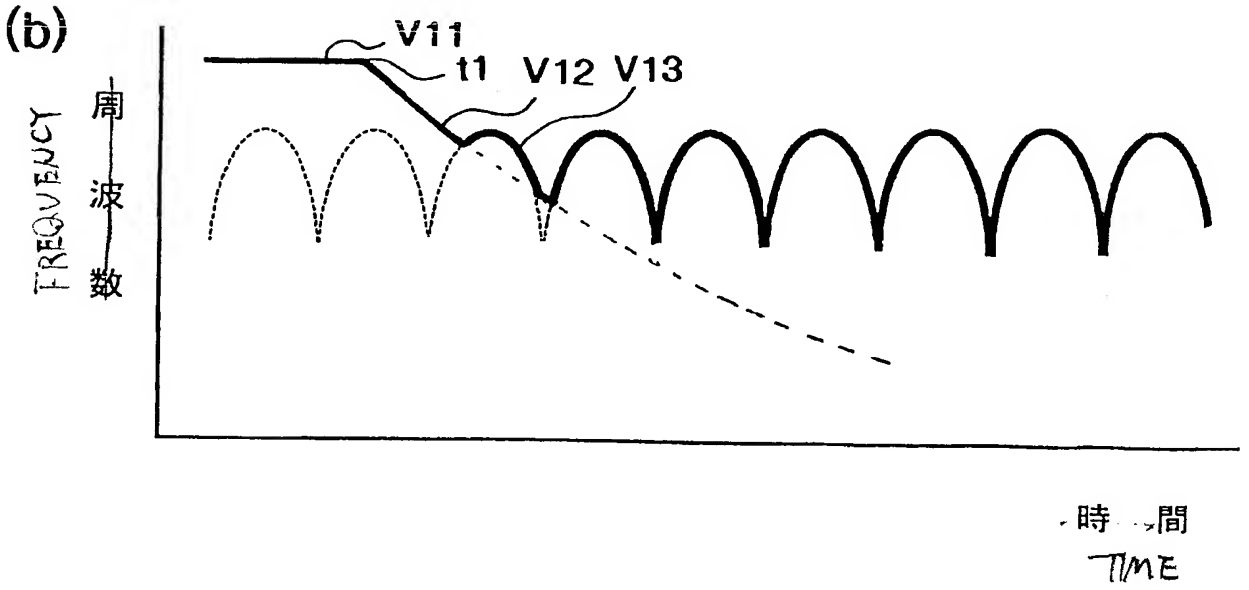

V11
t1
V12
V13
FREQUENCY
周波数
時間
TIME

Fig. 7

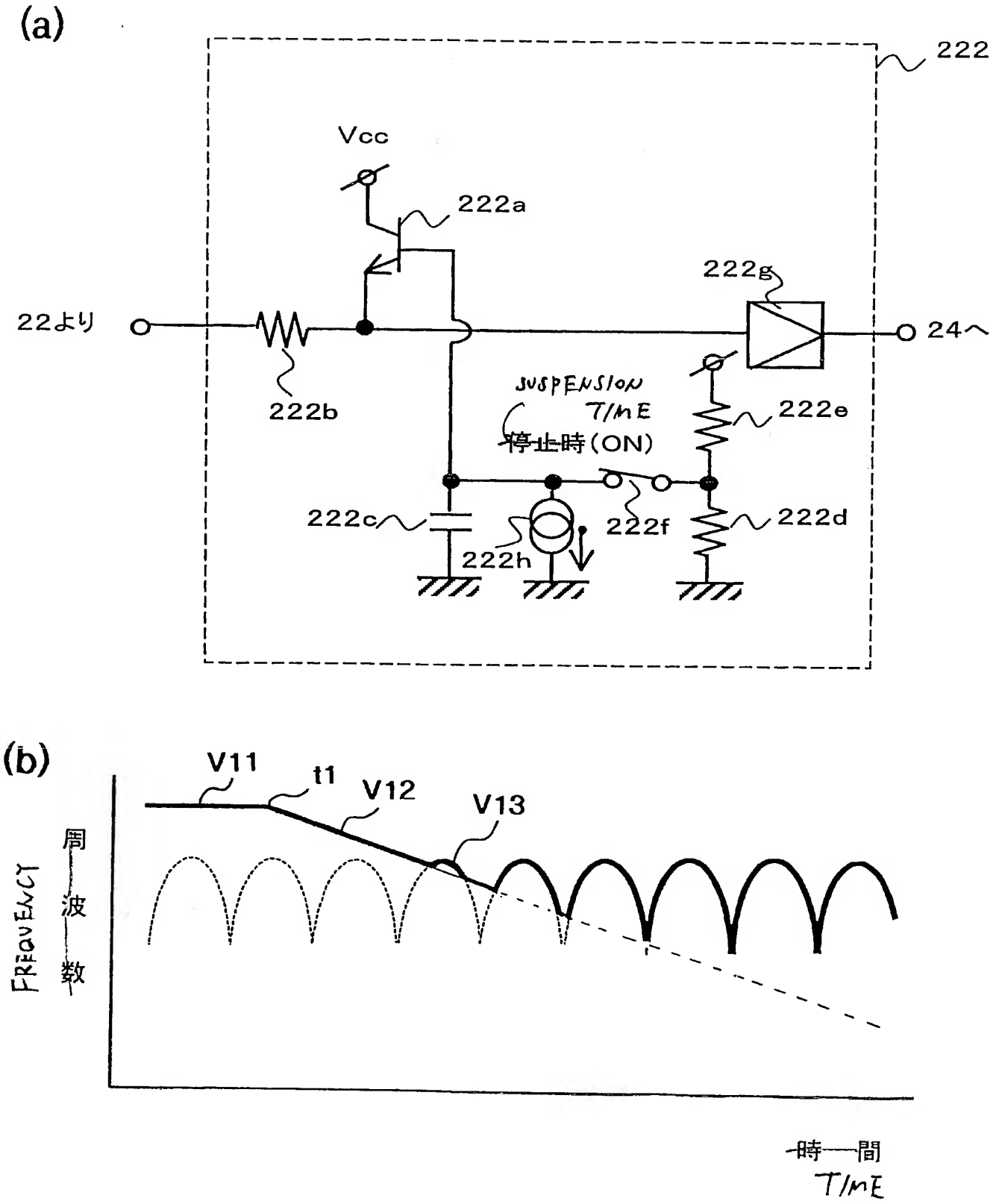

(a)
222
Vcc
222a
222g
22より
24へ
222b
SUSPENSION
TIME
停止時(ON)
222e
222c
222f
222d
222h
(b)
V11
t1
V12
V13
FREQUENCY
周波数
時間
TIME

Fig. 8

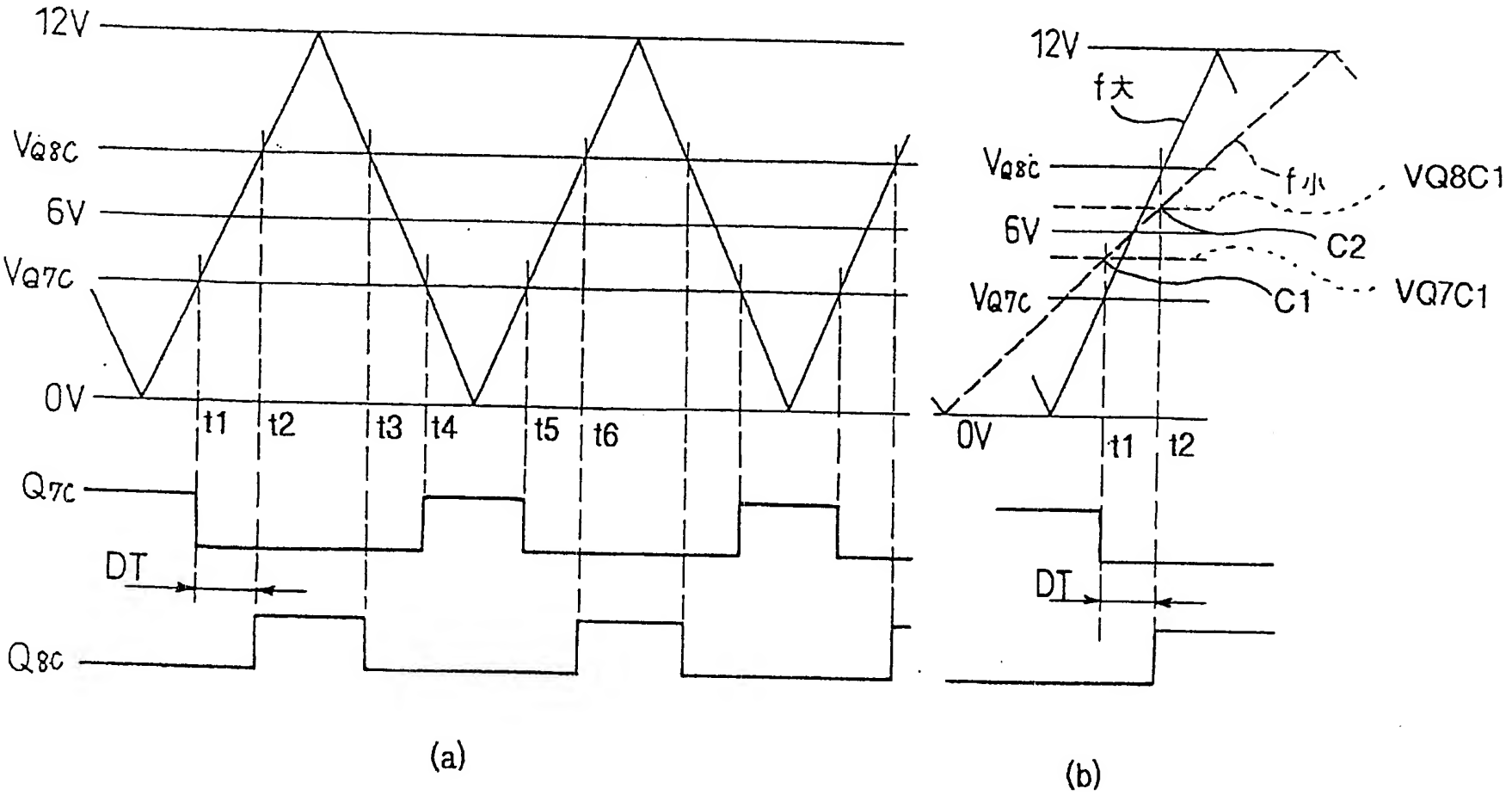

12V
VQ8C
6V
VQ7C
0V
t1
t2
t3
t4
t5
t6
Q7C
DT
Q8C
(a)
12V
f大
VQ8C
f小
VQ8C1
6V
C2
VQ7C
C1
VQ7C1
0V
t1
t2
DT
(b)

Fig. 9

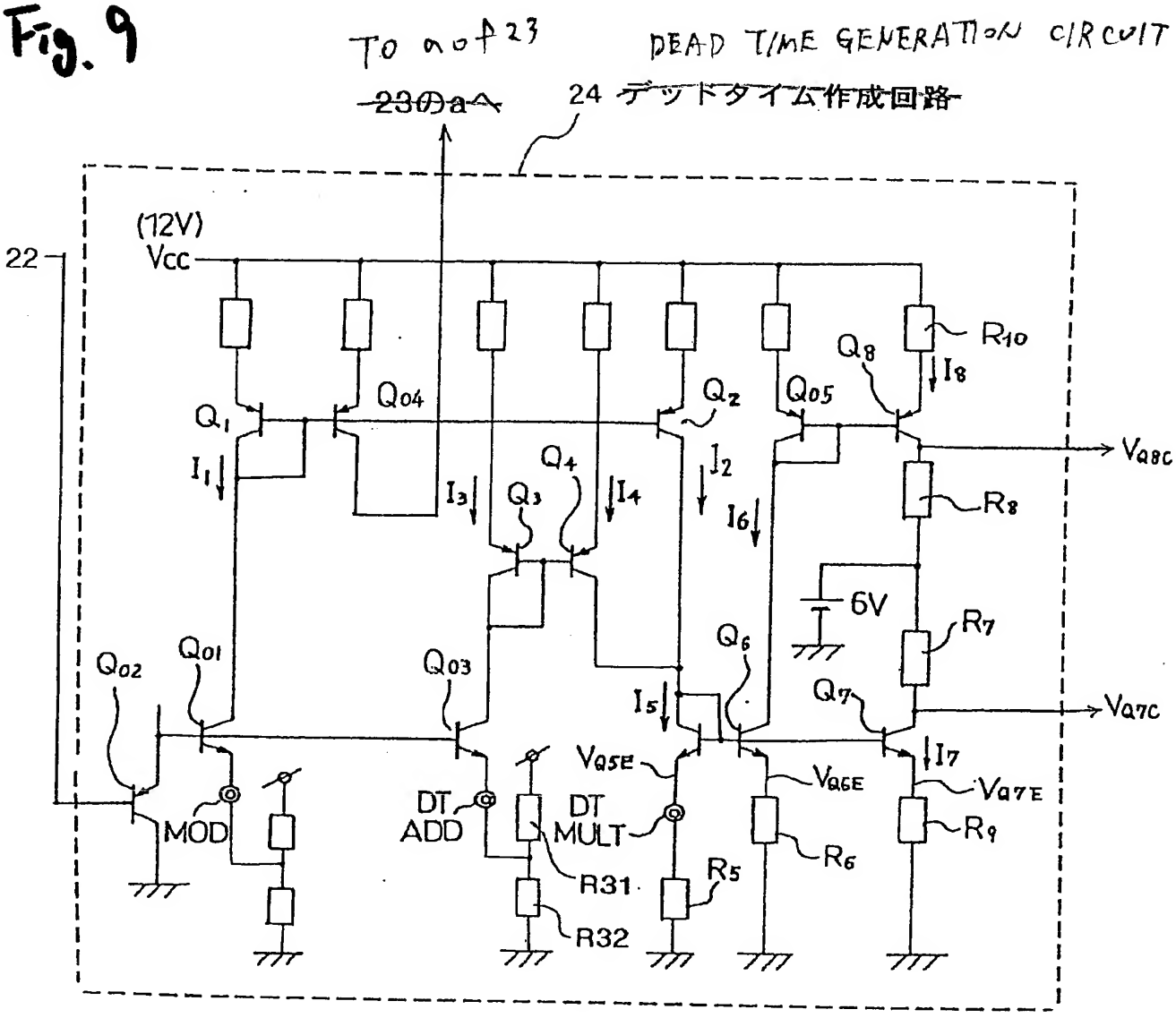

TO ~~230a~~ of 23
DEAD TIME GENERATION CIRCUIT
~~230a~~
24 ~~デッドタイム作成回路~~
22
(12V)
Vcc
Q1
Q04
Q2
Q05
Q8
R10
I8
I1
I3
Q3
Q4
I4
I2
I6
VQ8C
R8
6V
R7
Q02
Q01
Q03
Q6
I5
Q7
VQ7C
I7
VQ5E
VQ6E
VQ7E
DT
ADD
DT
MULT
MOD
R31
R32
R5
R6
R9

Fig. 10

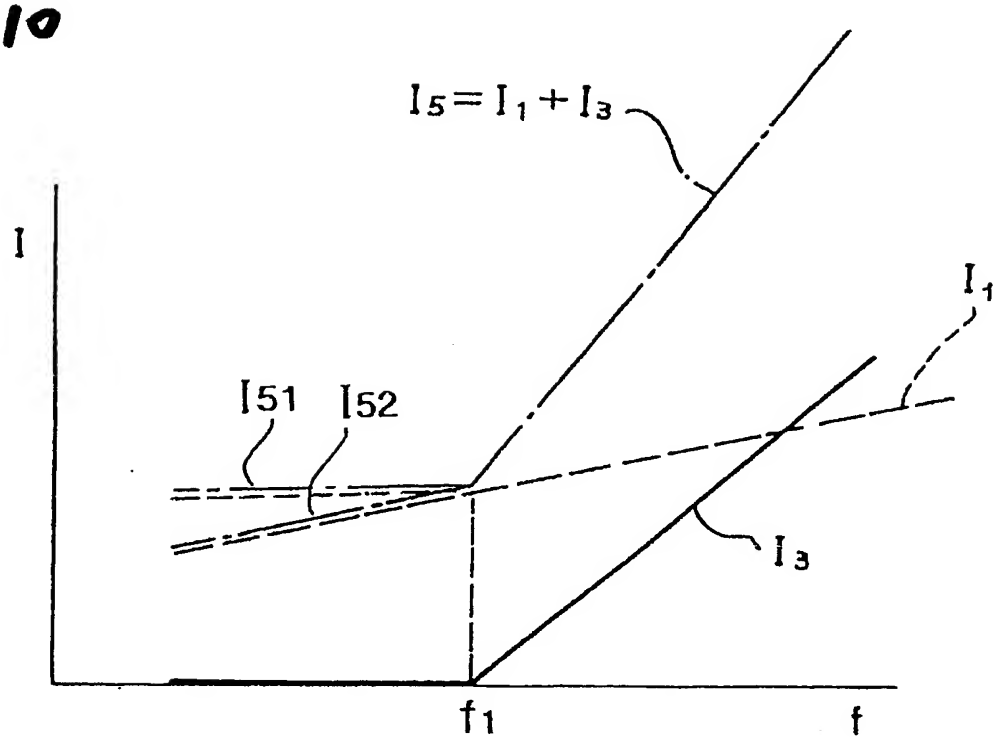


Fig. 11

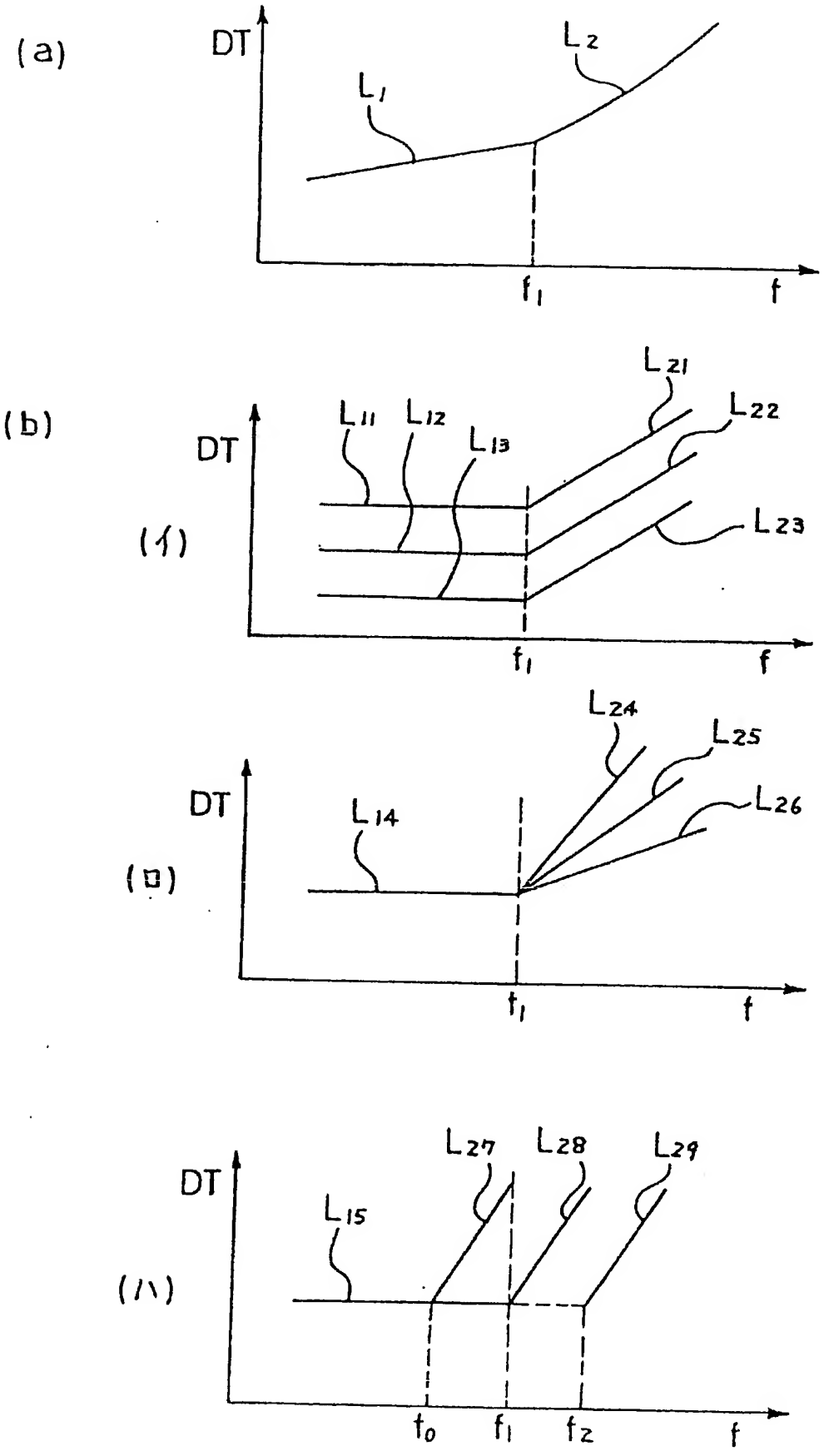

(a)
DT
L1
L2
f1
f
(b)
(1)
DT
L11
L12
L13
L21
L22
L23
f1
f
(2)
DT
L14
L24
L25
L26
f1
f
(3)
DT
L15
L27
L28
L29
t0
f1
f2
f

Fig. 12

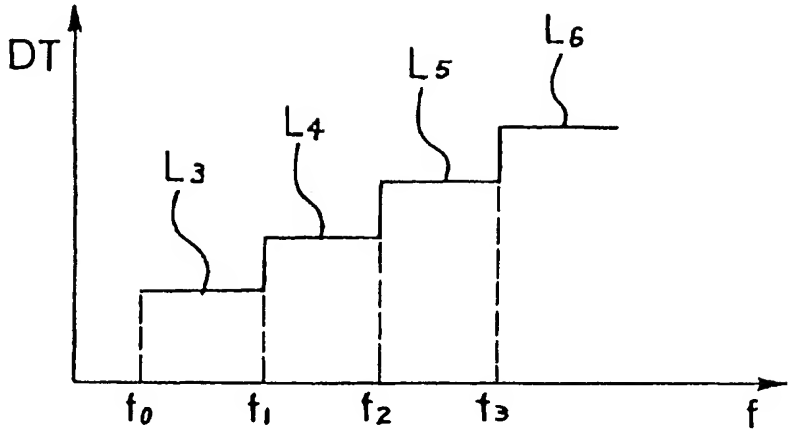


Fig. 13

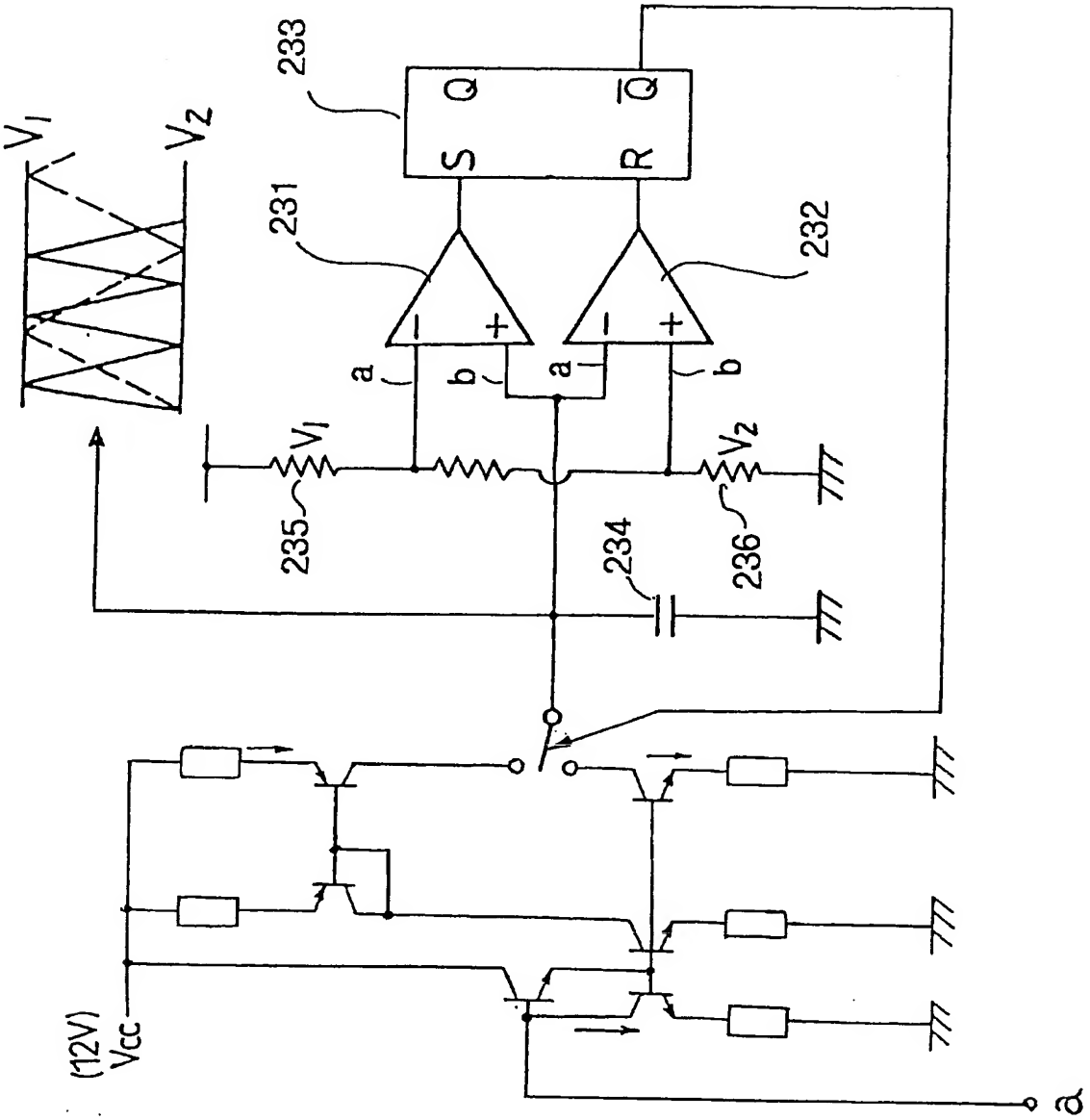
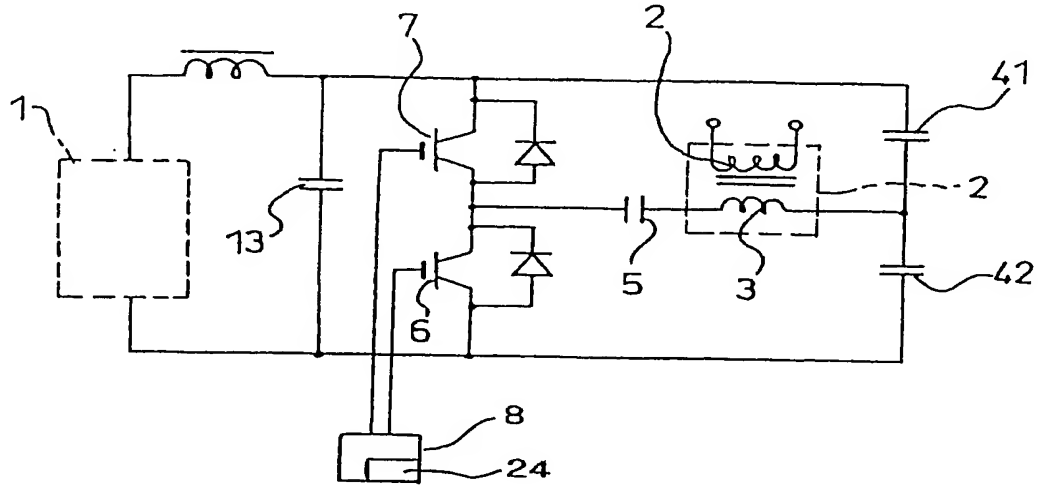
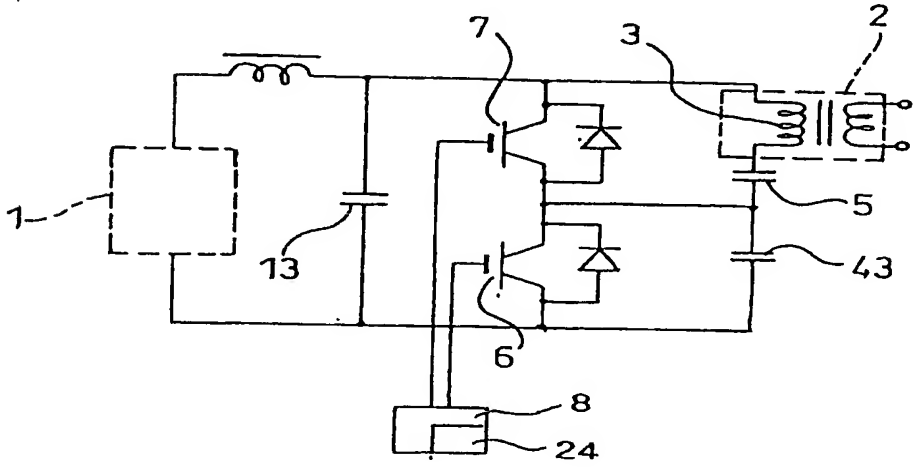

23
233
Q
$\overline{Q}$
S
R
231
232
V_1
V_2
a
b
a
b
V_1
V_2
235
234
236
(12V)
Vcc
a

Fig. 14

(a)



(b)



(C)

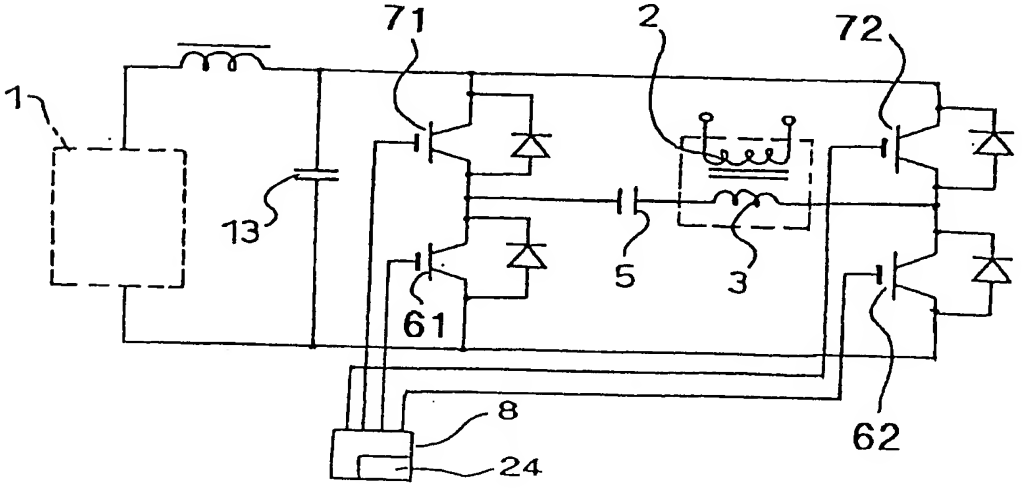


Fig. 15

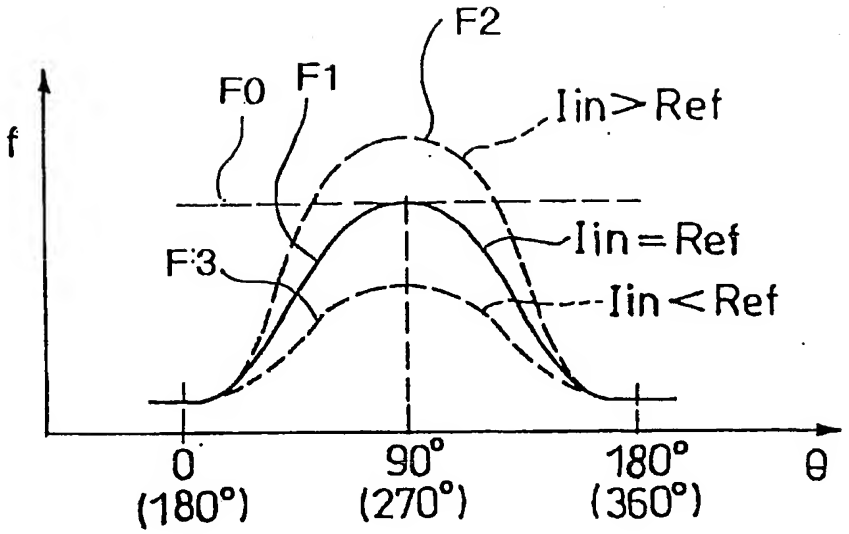
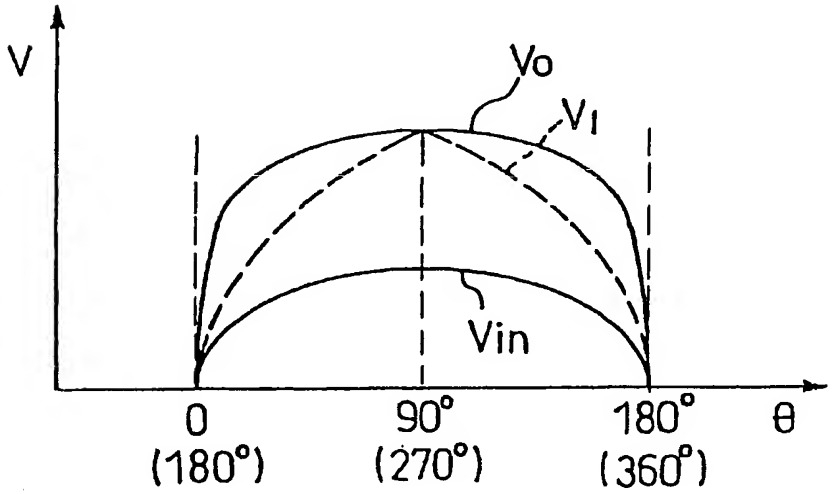

F2
F0
F1
Iin>Ref
f
Iin=Ref
F3
Iin<Ref
0
(180°)
90°
(270°)
180°
(360°)
θ

Fig. 16


V
Vo
V1
Vin
0
(180°)
90°
(270°)
180°
(360°)
θ